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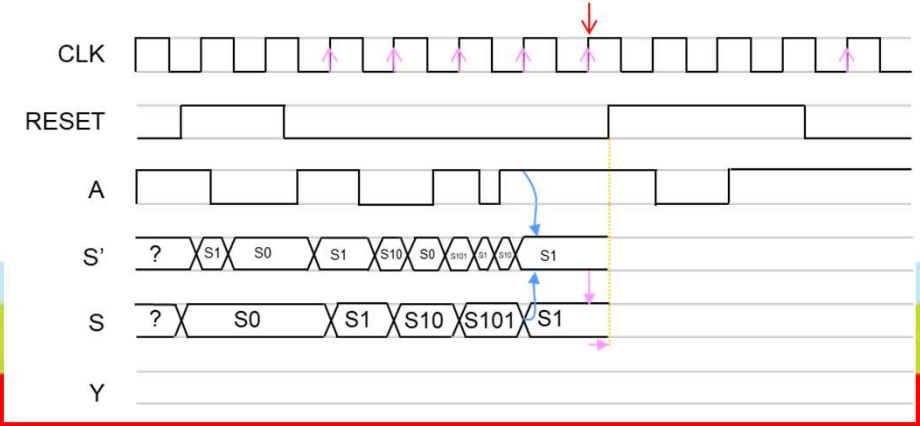
Timing diagrams of Finite State Machines



Gabriel Caffarena
Departamento de Tecnologías de Información
Universidad San Pablo CEU
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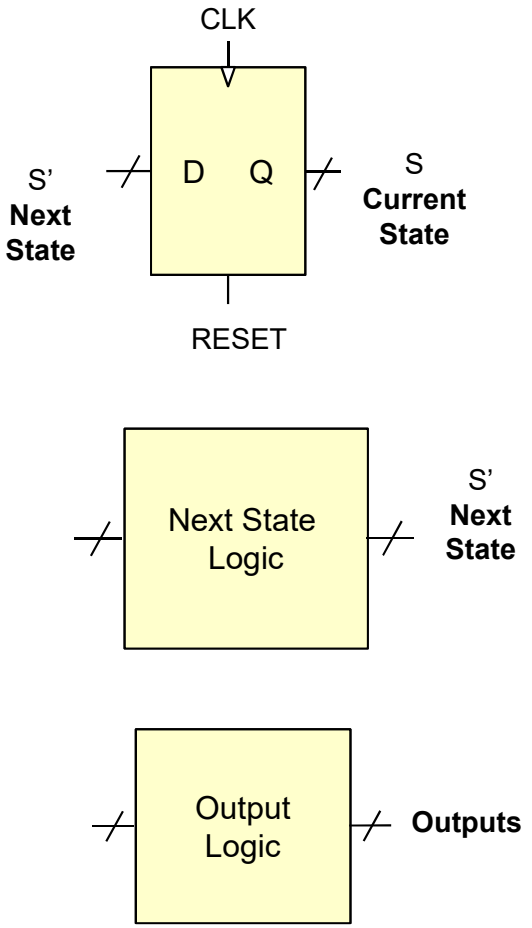
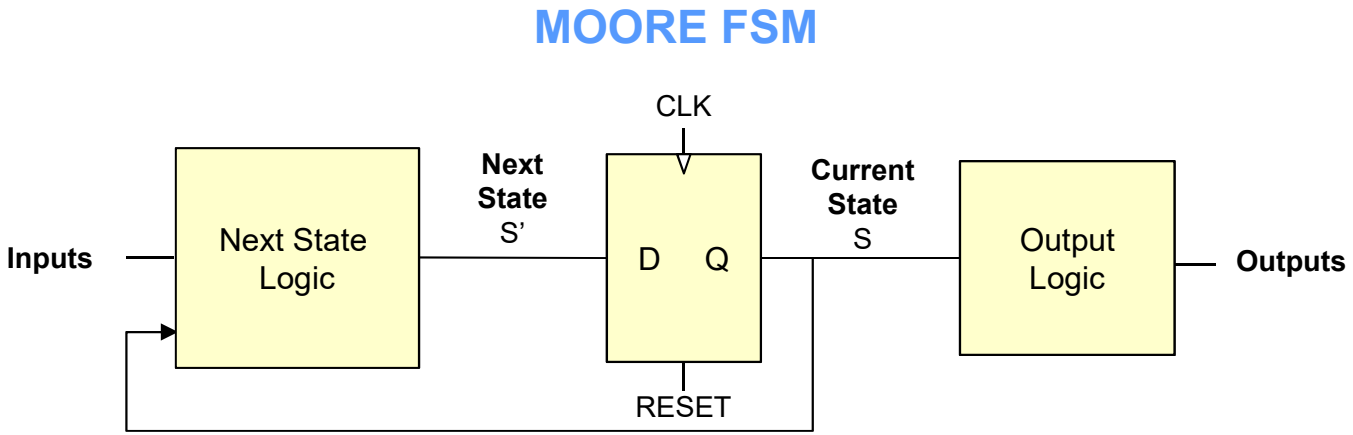
Finite State Machine (FSM)

- Used to generate a sequence of control signals that react to the value of inputs
  - The sequence is synchronous with a periodic clock signal
- Consists of:
  - State register that
    - Store the current state and
    - Load the next state at the clock edge
  - Combinational logic that
    - Computes the next state
    - Computes the outputs



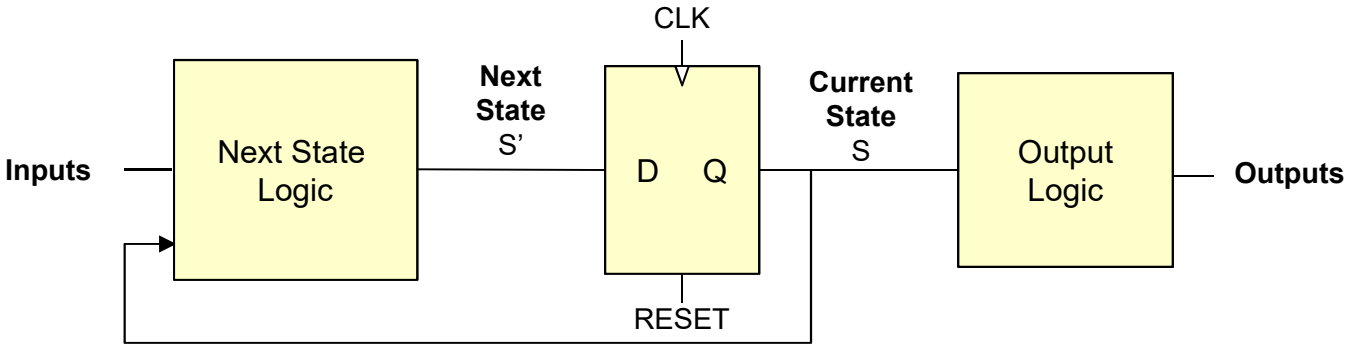
Finite State Machines (FSMs)

- Next state is determined by the current state and the inputs
- There are two types of finite state machines depending on the output logic:
  - **Moore FSM**: the outputs depend **o**nly on the current state (Edward F. Moore, 1956)
  - Mealy FSM: outputs depend on the current state *and* the inputs (George H. Mealy, 1955)



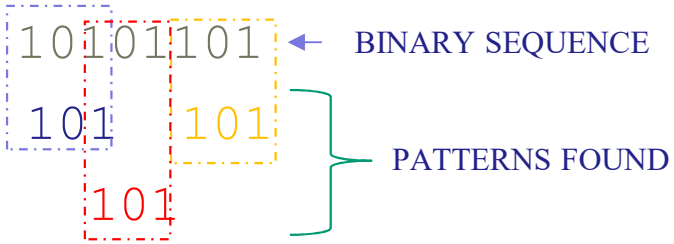
Moore Finite State Machines

- Let's analyze the block diagram
  - The RESET signal resets the state to the initial state (i.e. S0)
  - When a clock Edge accurs S=S'
  - The outputs are updated everytime S is updated
  - The next state S' is updated if S if update and/or the inputs change

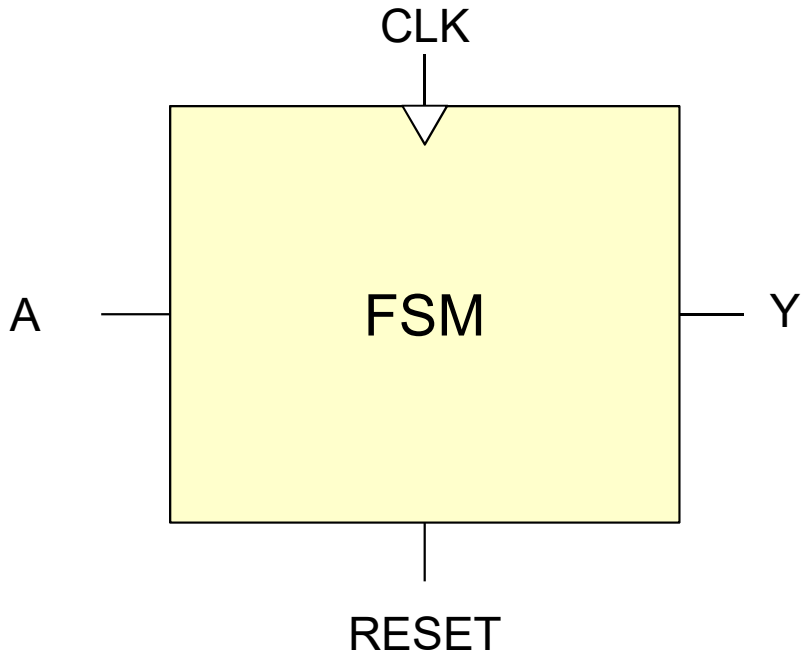


FSM example

- System that reads a binary sequence A and detect the pattern 101
- The end of one pattern can be the beggining of a new pattern

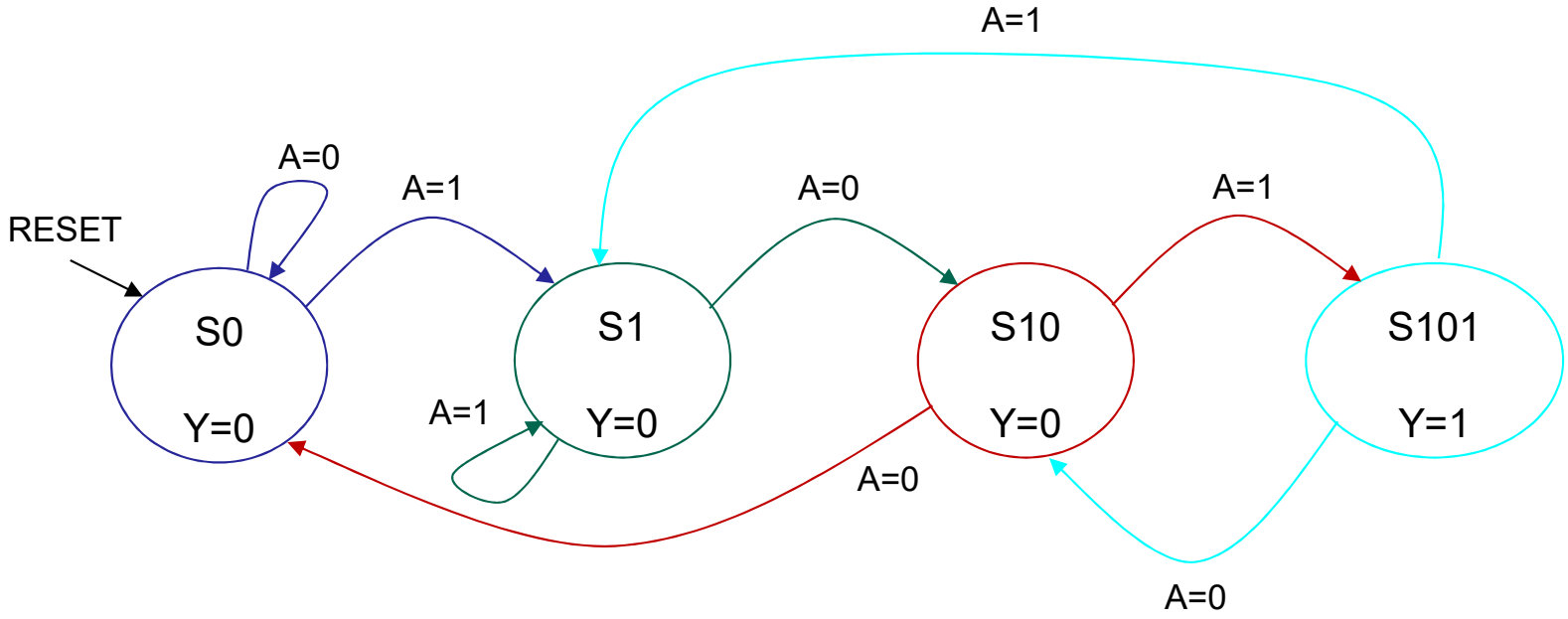


- Inputs: *CLK*, *Reset*, *A*
- Outputs: *Y*
  - 1 if pattern found



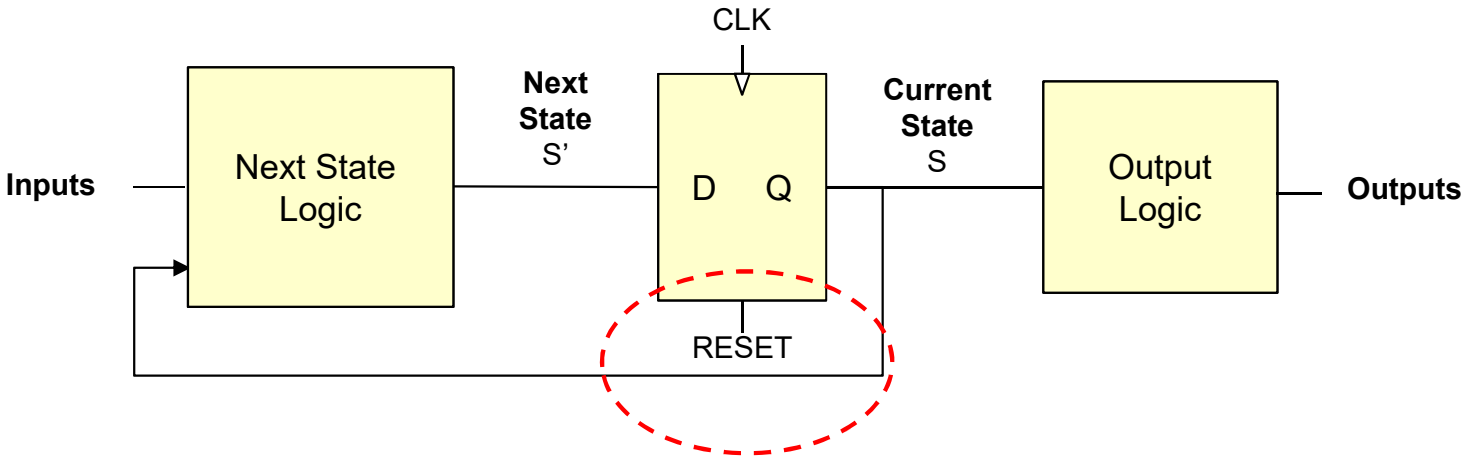
FSM State Transition Diagram

- Moore FSM: outputs labeled in each state
- States: Circles
- Transitions: Arcs



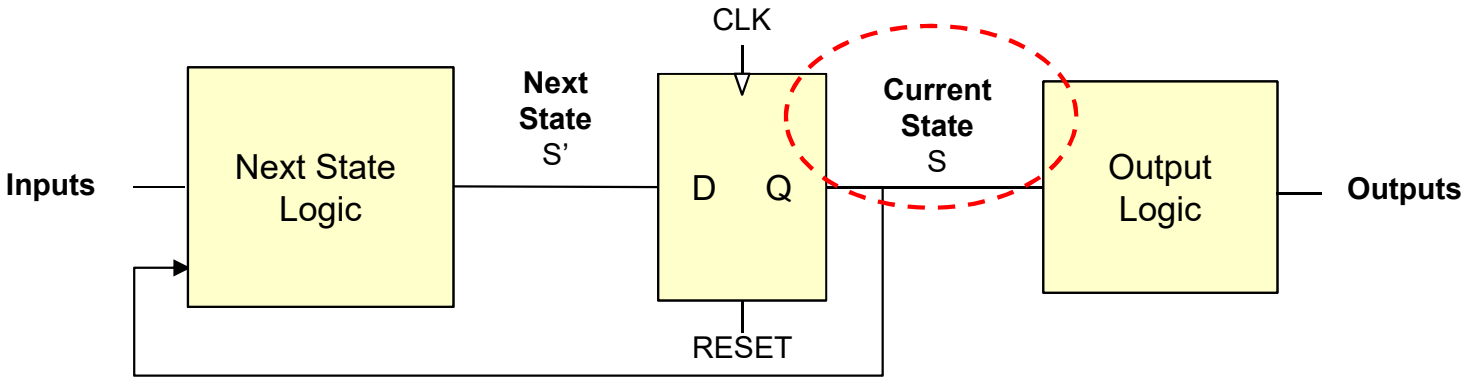
FSM Timing Diagram: Steps

- Reset
  - We assume that the reset signal is active high, that is:
    - If RESET=1 then the output of the register is all zeros, so S=S0, being S0 the initial state.
    - IF RESET=0 the value of the output of the register will be kept until a clock edge (transition from 0 to 1) occurs, and the value of S will be replaced by S' for a whole clock period



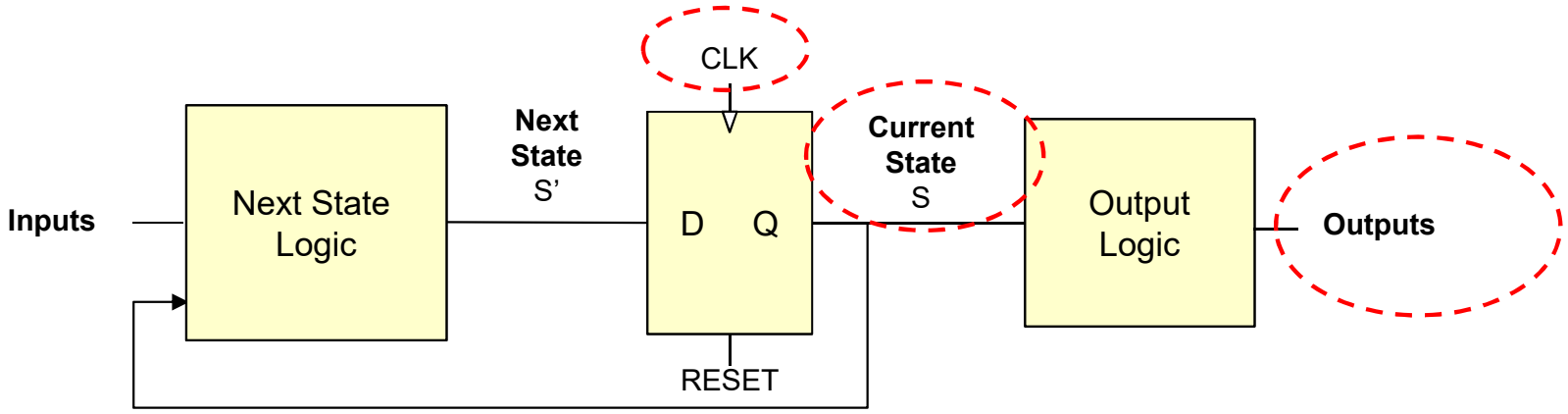
FSM Timing Diagram: Steps

- Clock edge (assuming that RESET=0)
  - We assume that the register react to rising clock edges (edge from 0 to 1) :
    - S=S' just after the clock edge (there will be a minor delay due to the propagation time of the registers that we will consider negligible).



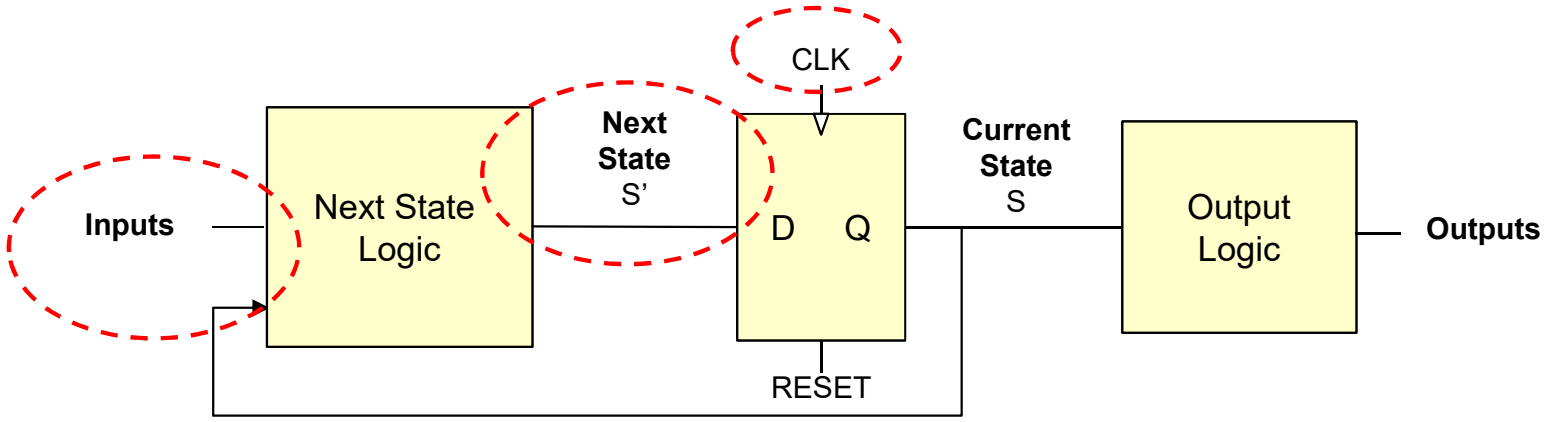
FSM Timing Diagram: Steps

- After the clock edge (assuming that RESET=0)
  - If S changed then the outputs might change depending on the current state (see state transition diagram)
  - There will be a delay due to the propagation delay of the combinational logic of the “output logic” block



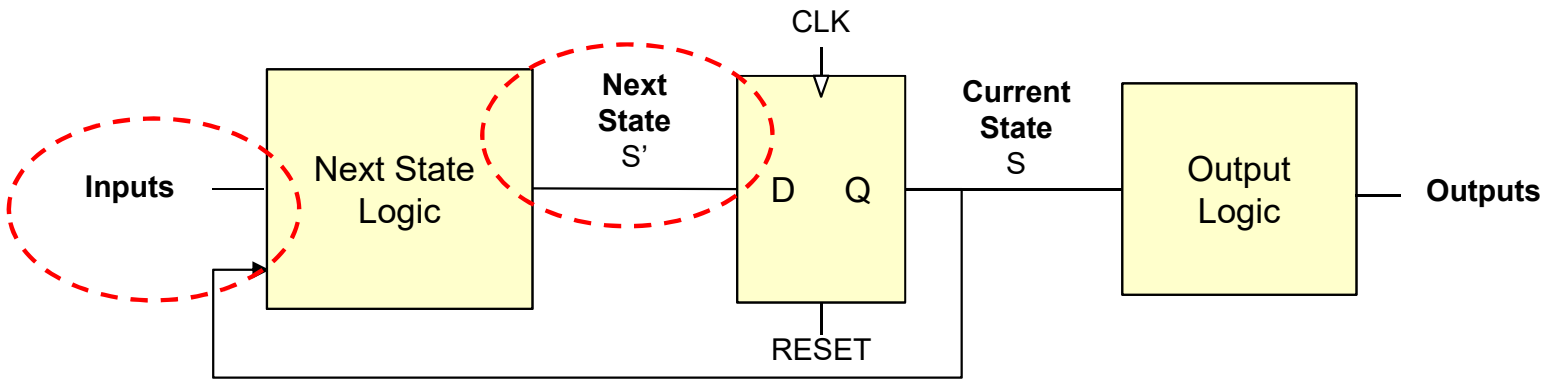
FSM Timing Diagram: Steps

- After the clock edge (assuming that RESET=0)
  - If S changed then the next state S' might change depending on the values of S and the inputs (see state transition diagram)
  - The change will have a delay due to the propagation delay of the combinational logic of the "next state logic" block



FSM Timing Diagram: Steps

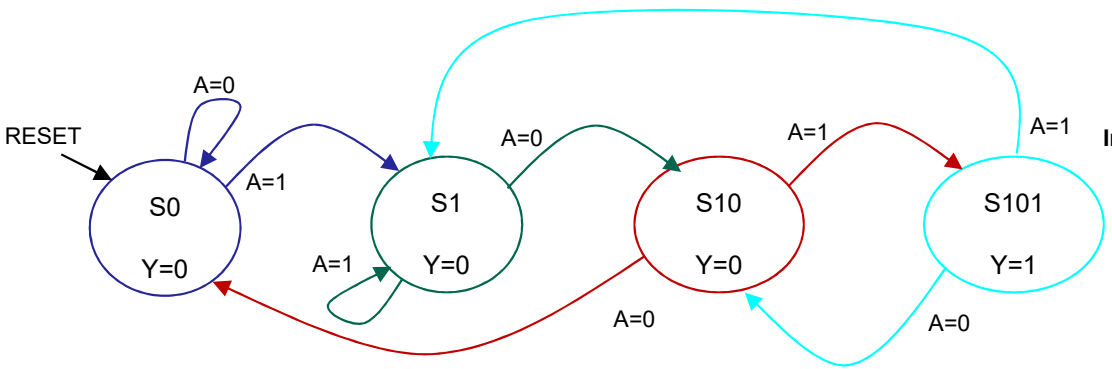
- Inputs
  - The inputs are not synchronized with the clock, so if the change S' might change depending on the values of S and the inputs (see state transition diagram)
  - The change will have a delay due to the propagation delay of the combinational logic of the "next state logic" block

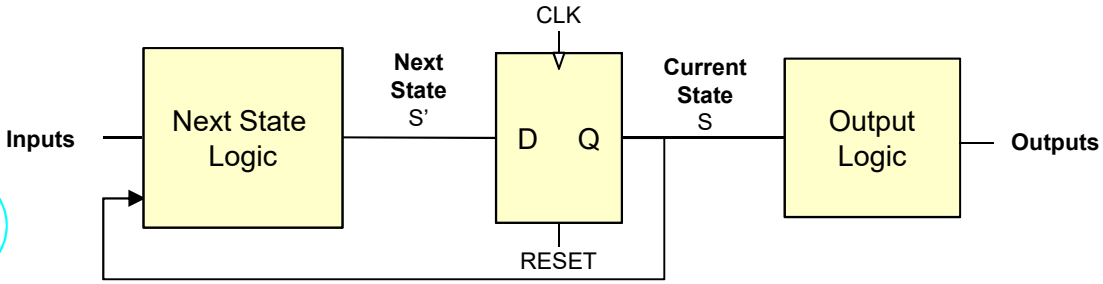


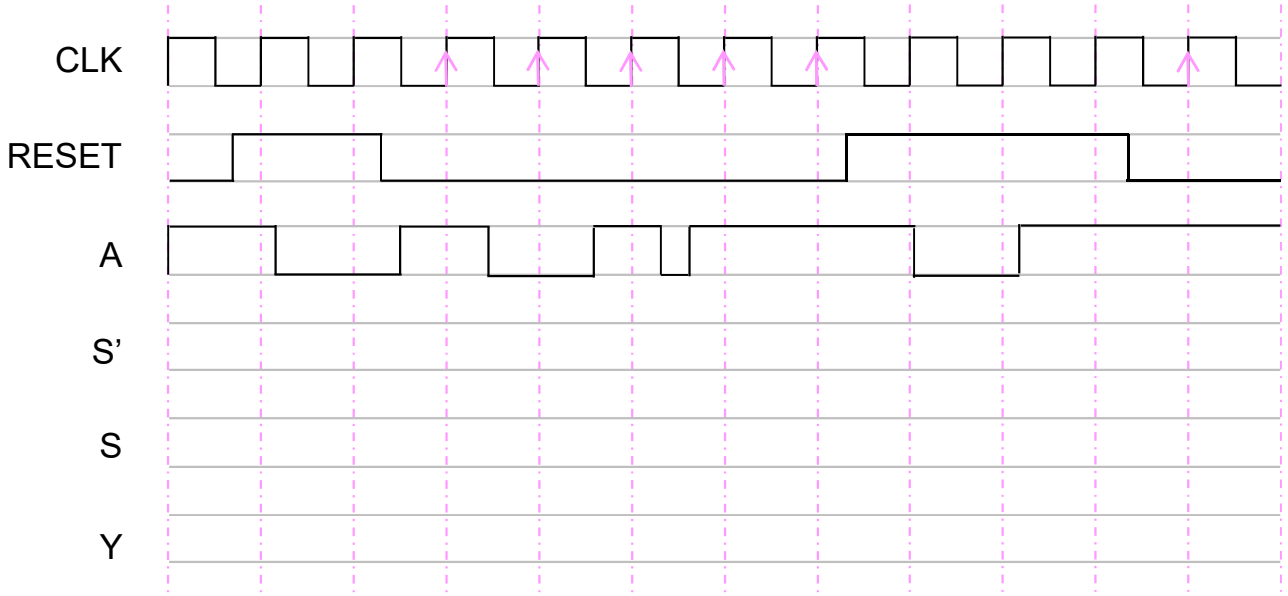
FSM Timing Diagram: Drawing the timing diagram

- In order to draw the timing diagram we require to specify the values of:
  - The clock and the reset signal
  - The inputs
- With that information and following the previous steps it will be possible to obtain the values of the outputs
  - It is necessary to obtain the value of S, which depends on the value of S'
  - S and S' must be part of the diagram
- Since the outputs are directly related to S we can leave them to the end and focus on S and S'

FSM Timing Diagram: Drawing the timing diagram







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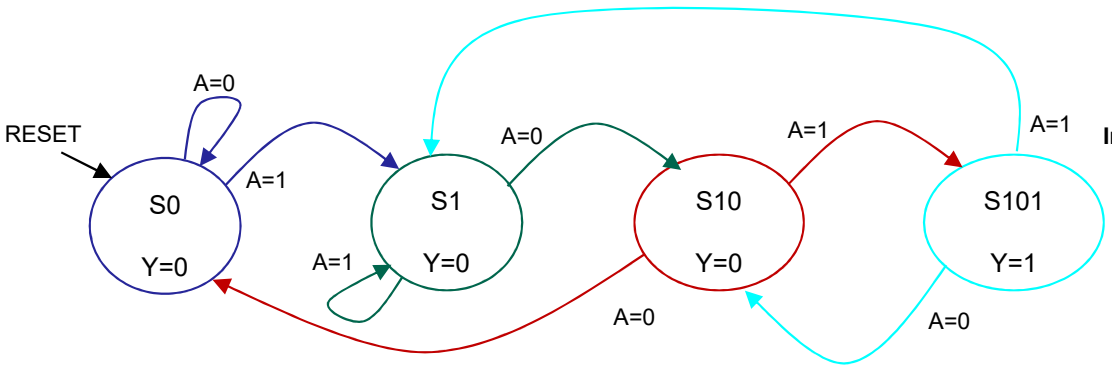

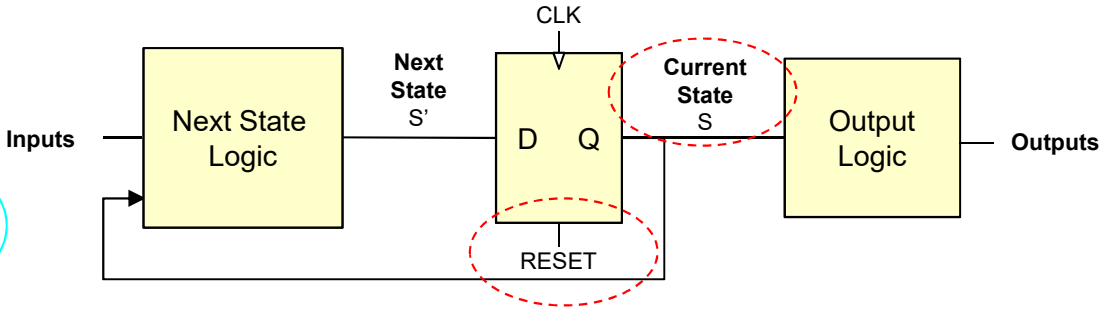

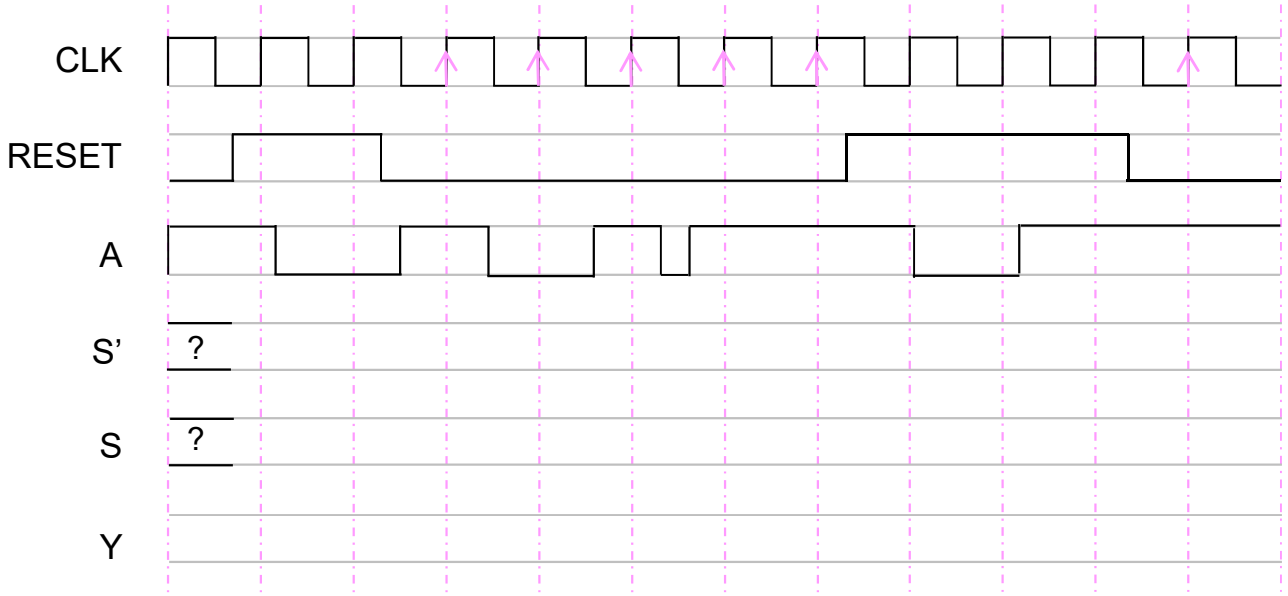

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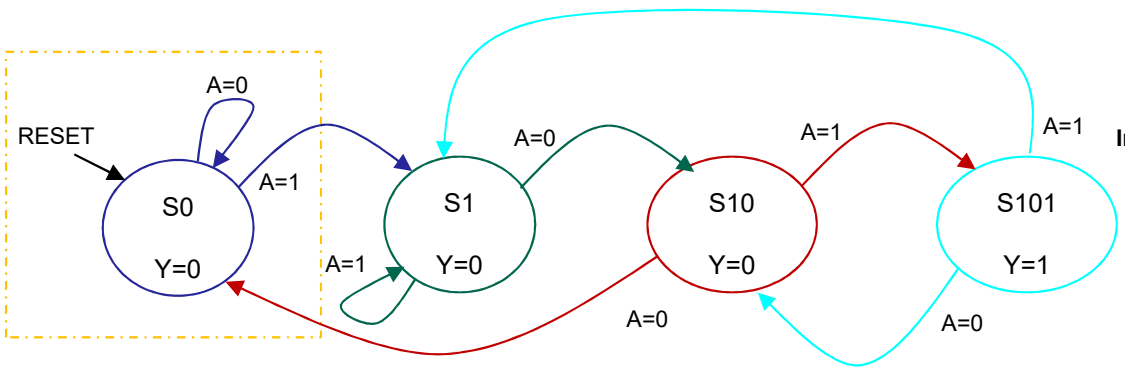

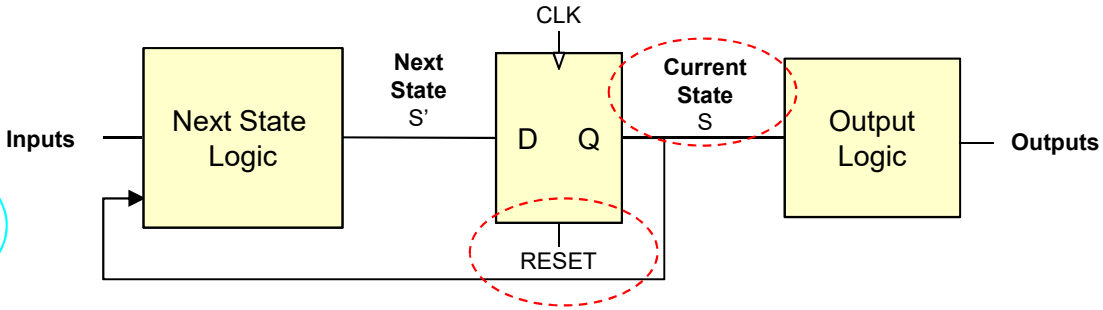

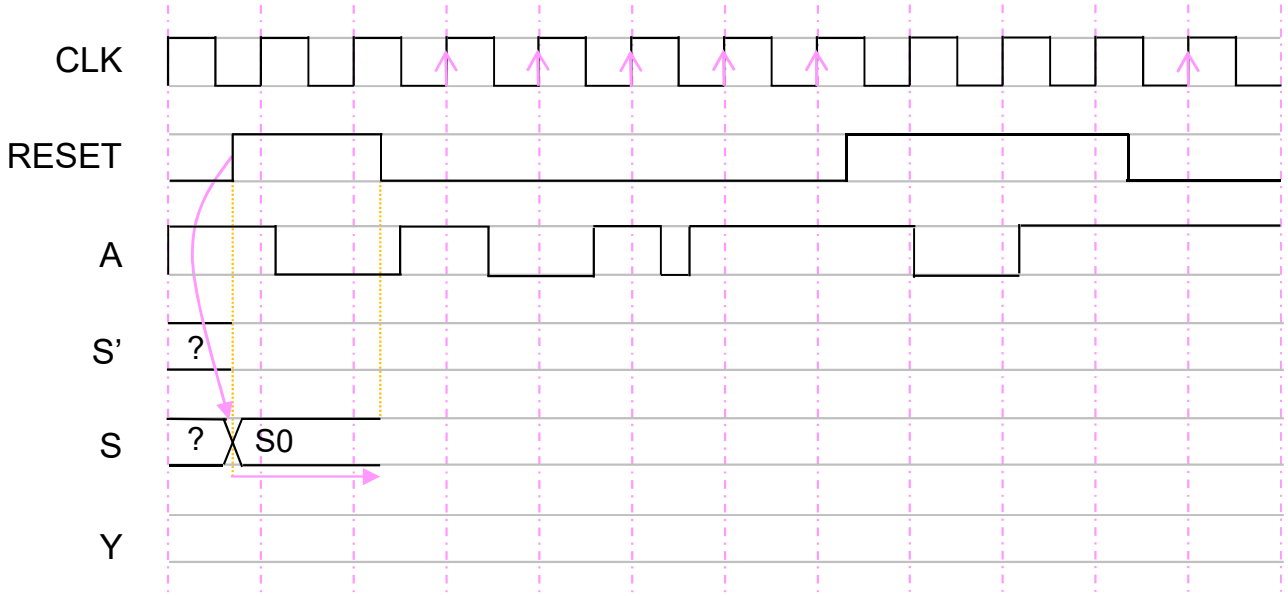

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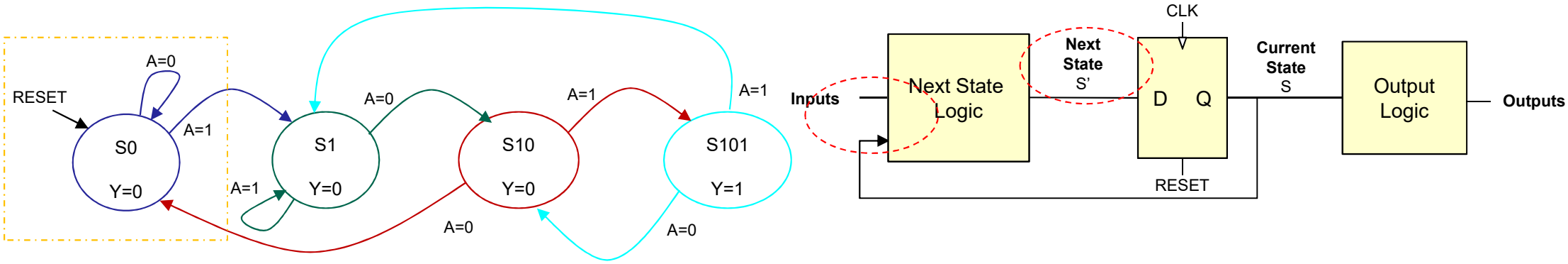

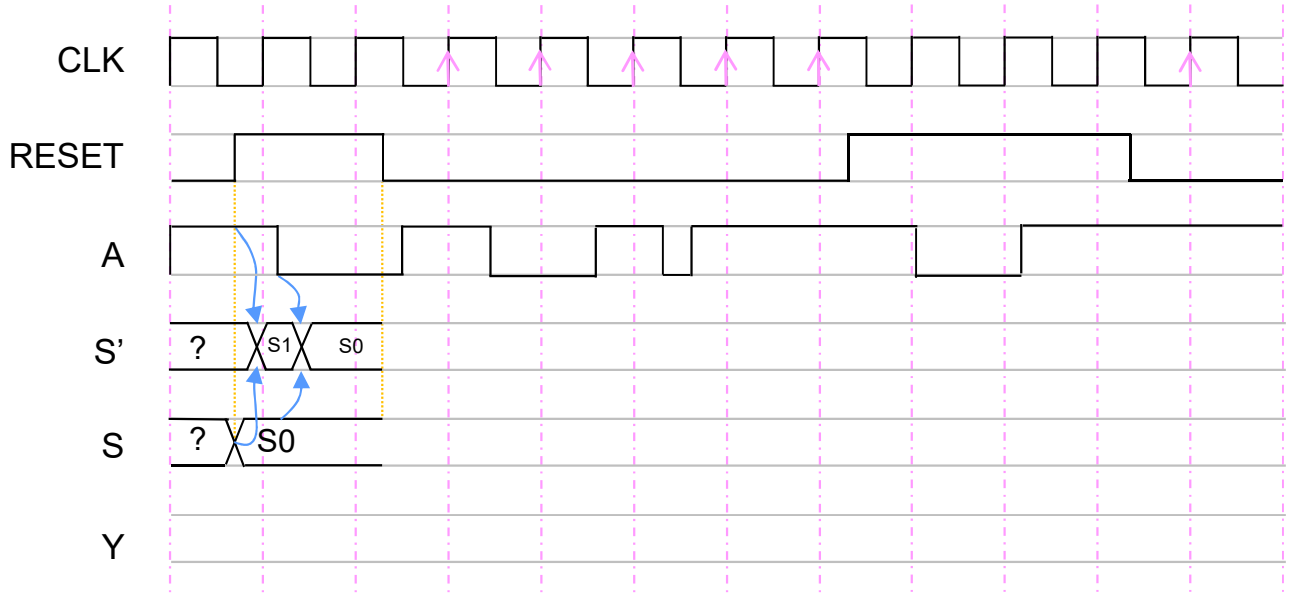

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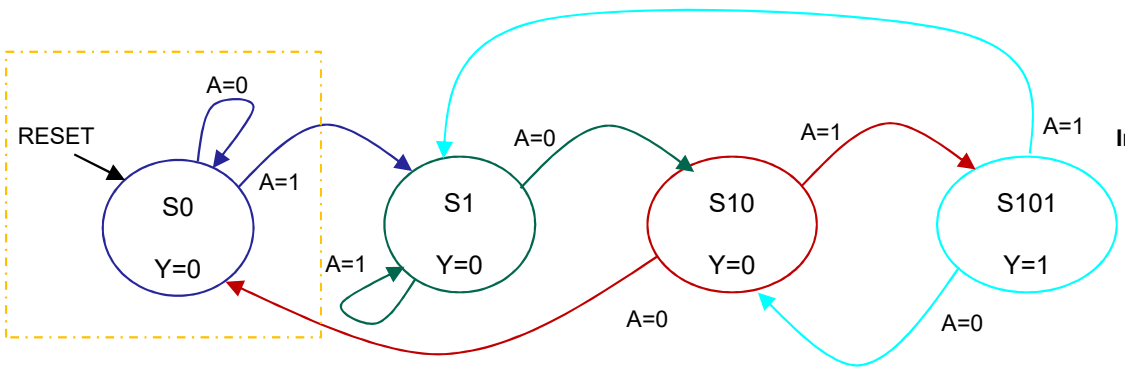

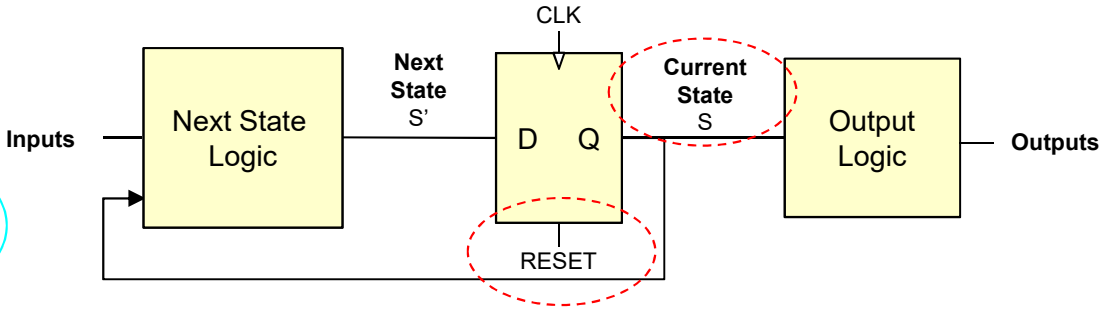

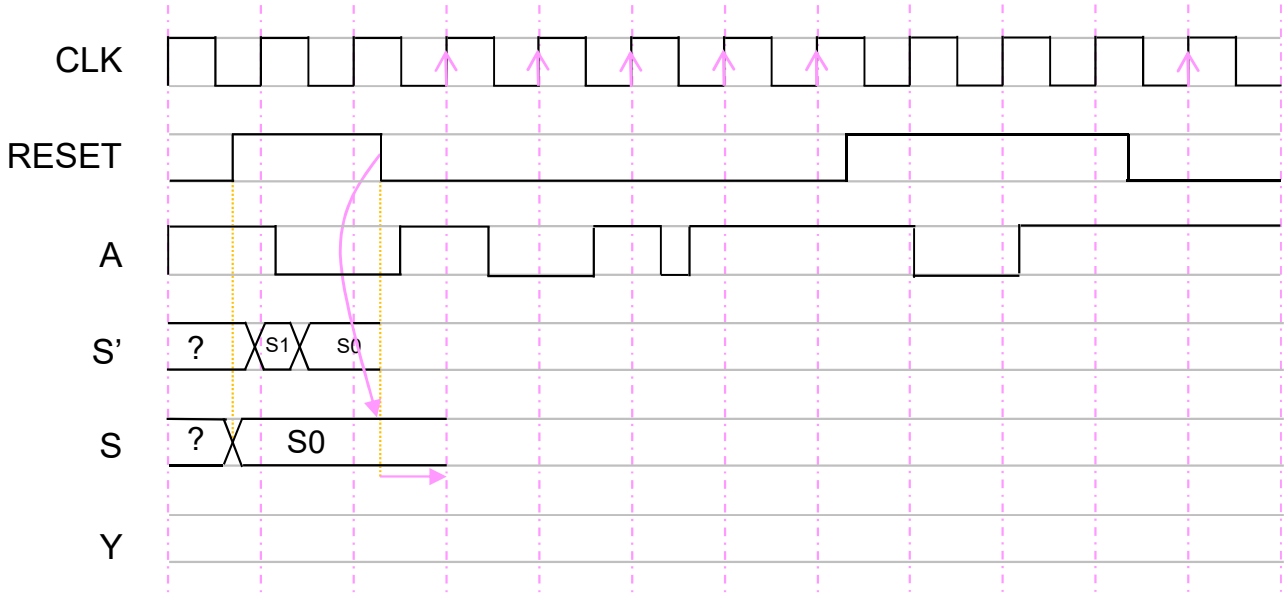

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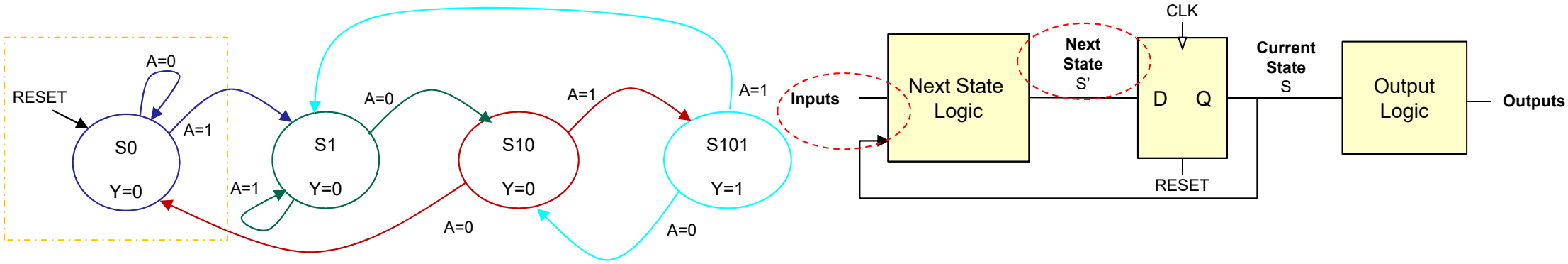

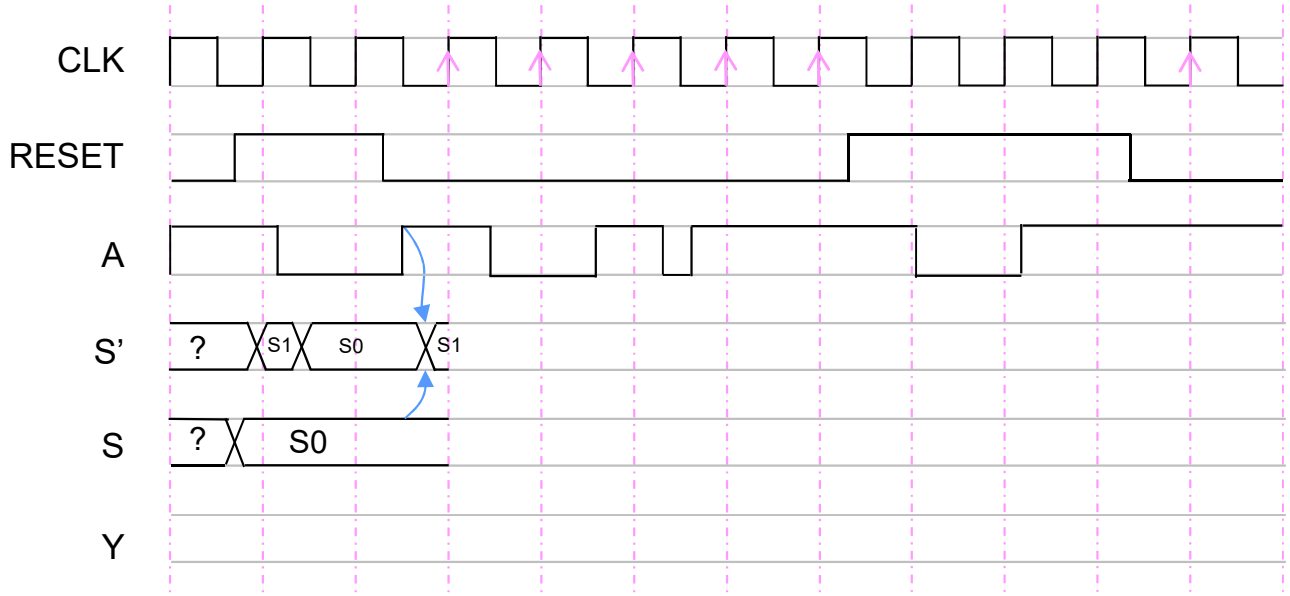

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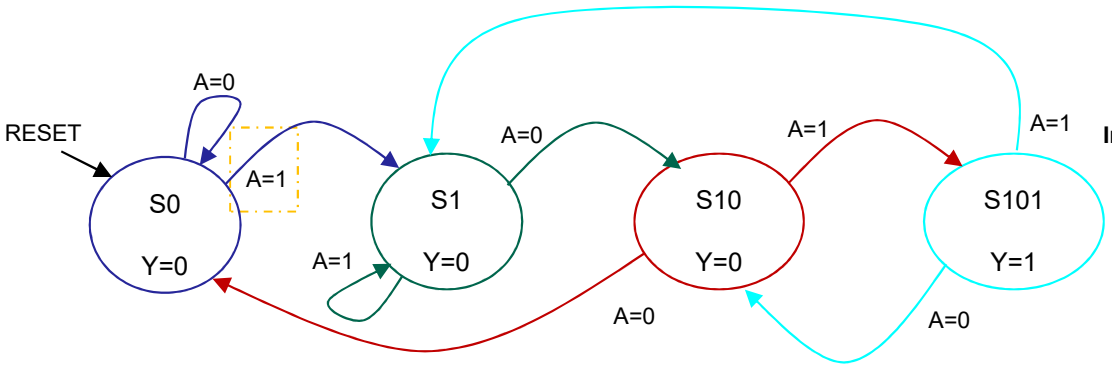

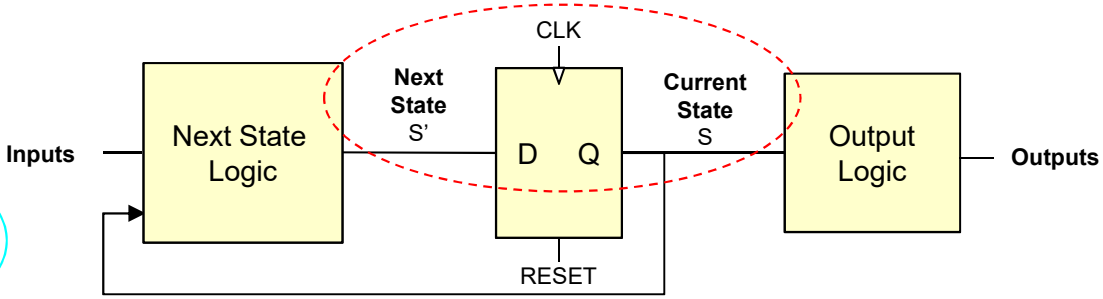

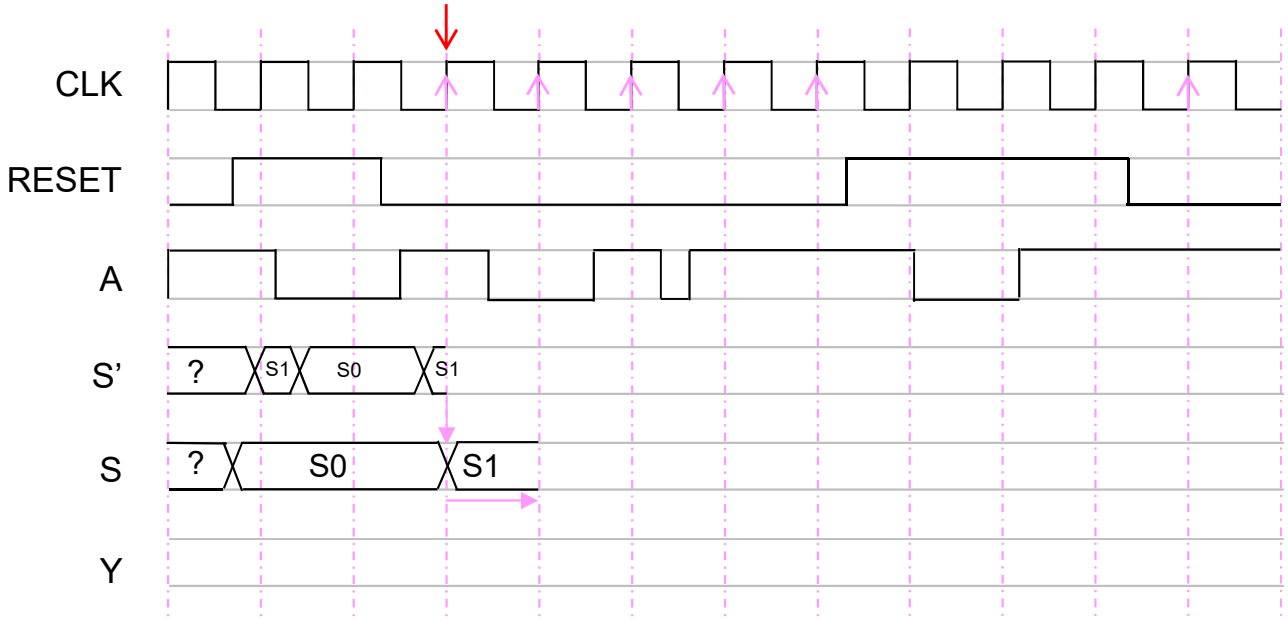

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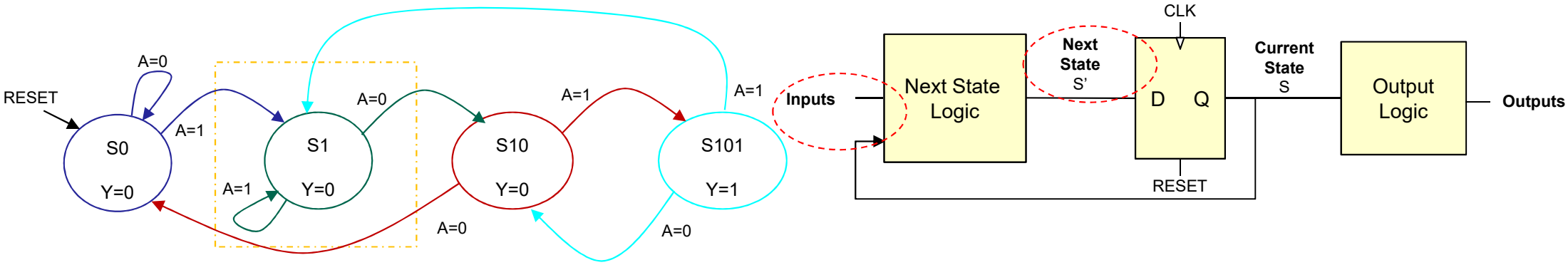

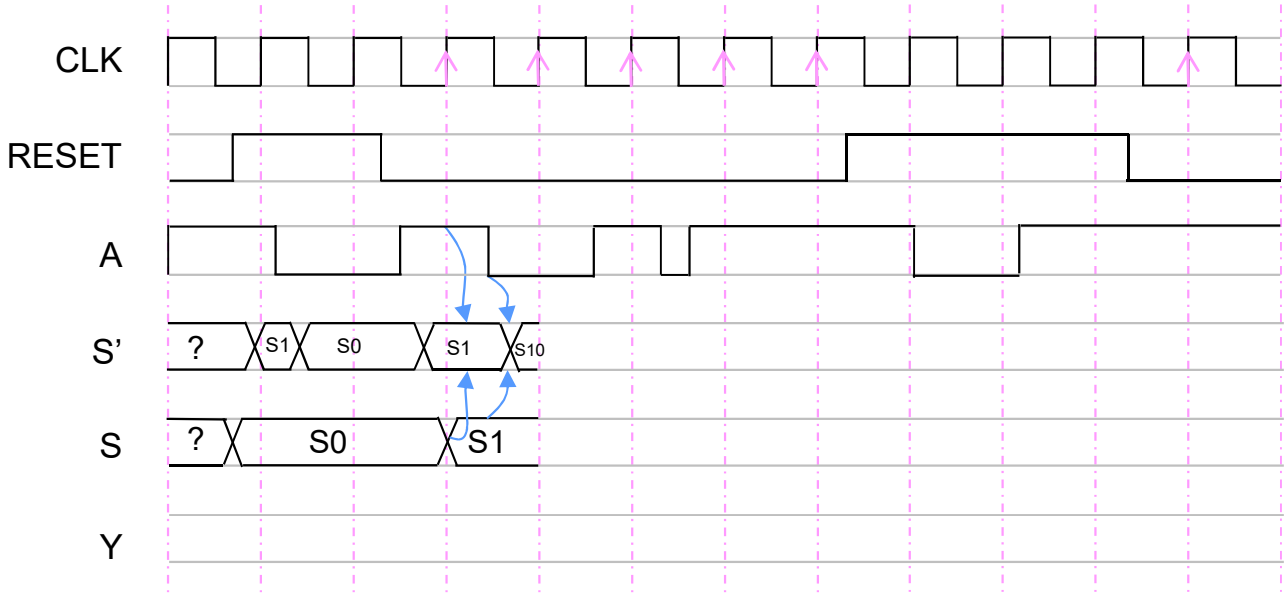

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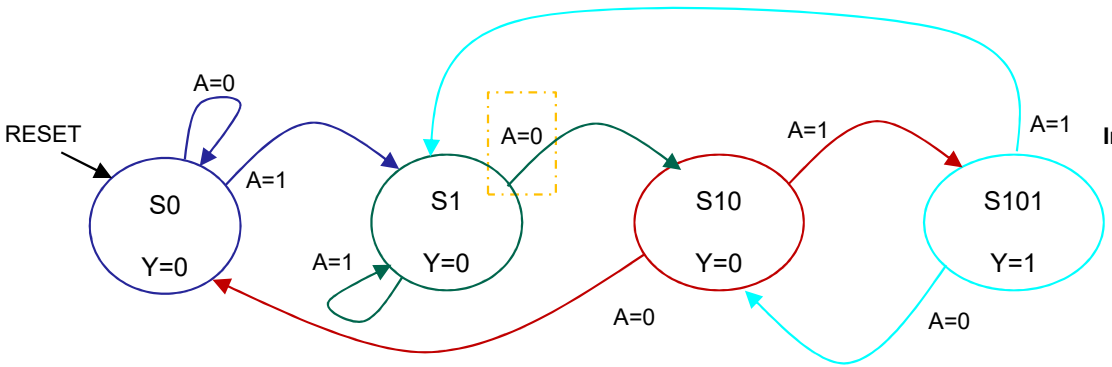

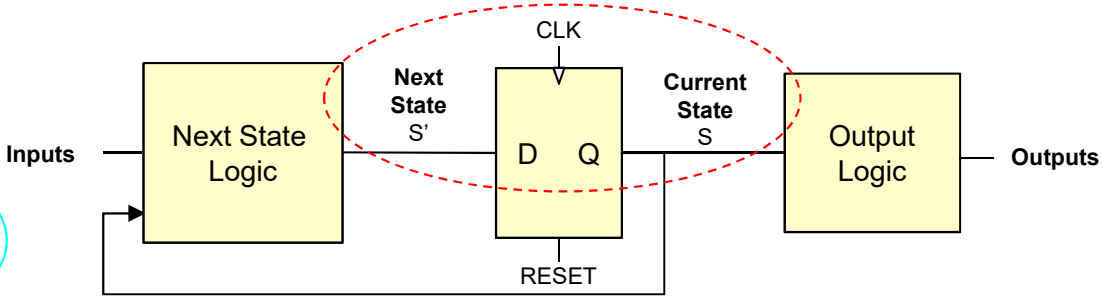

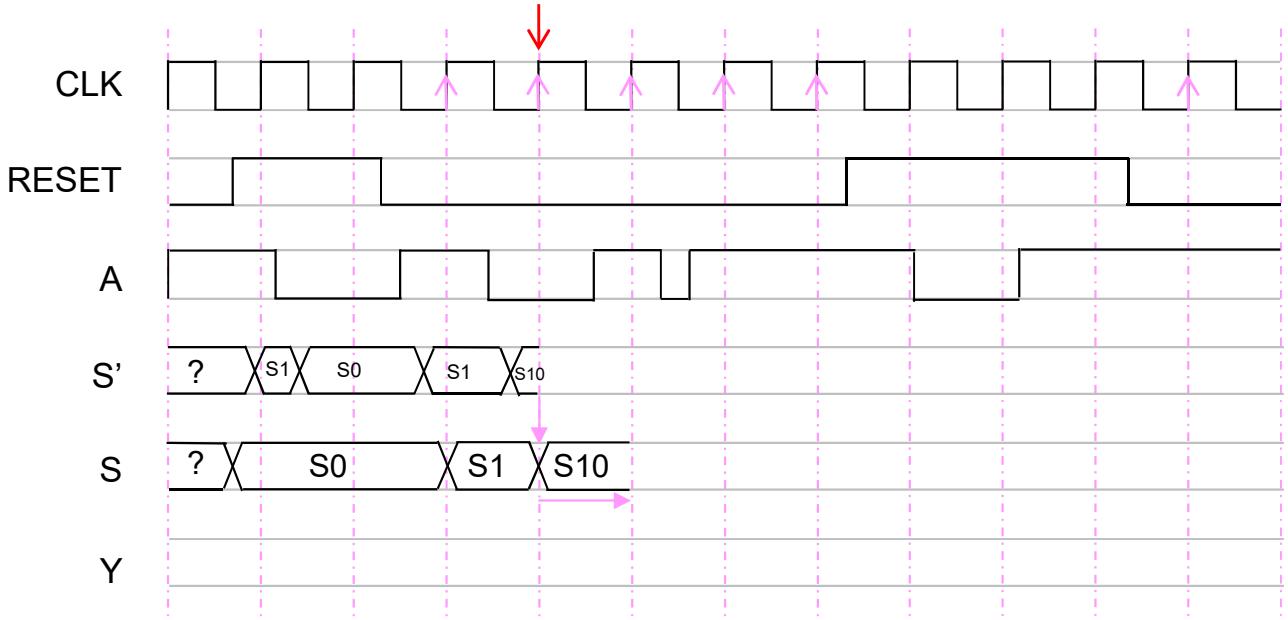

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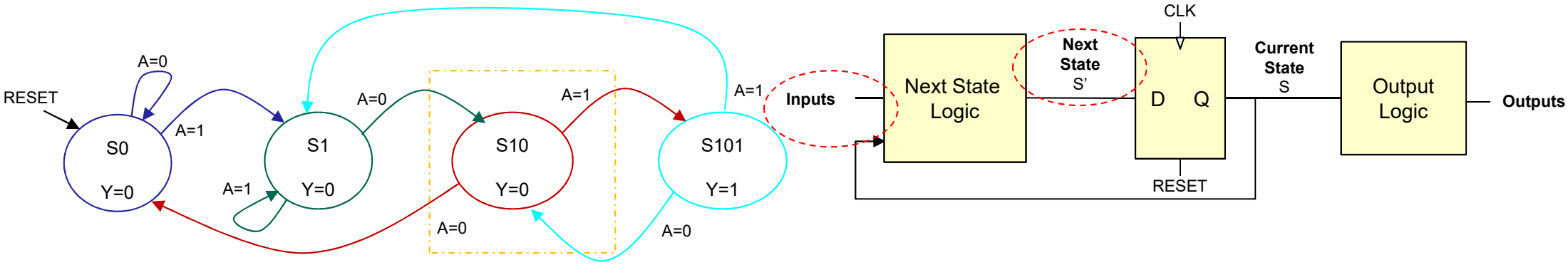

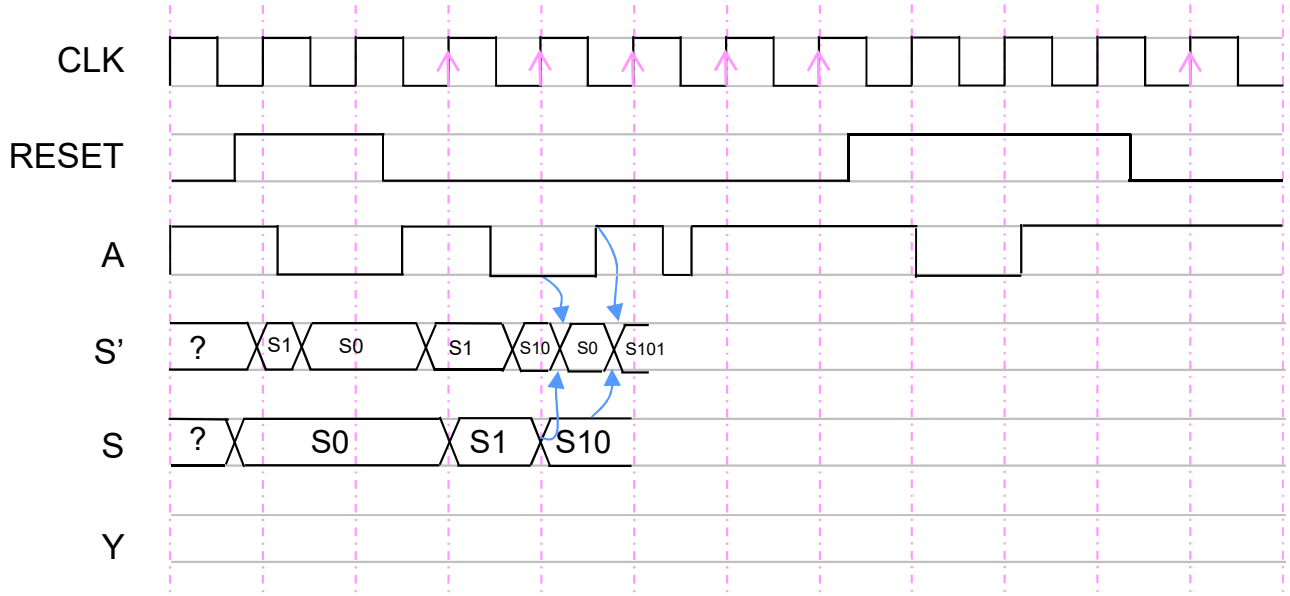

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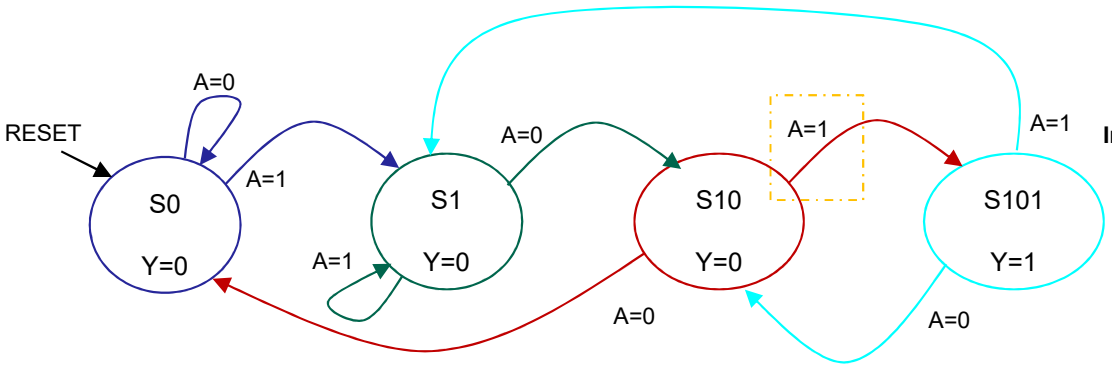

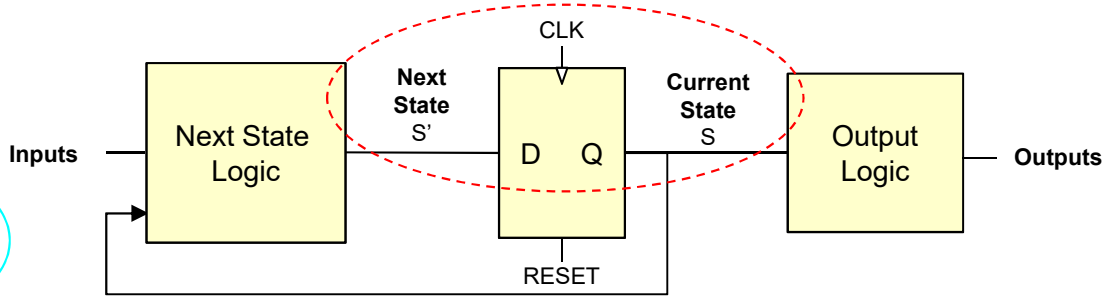

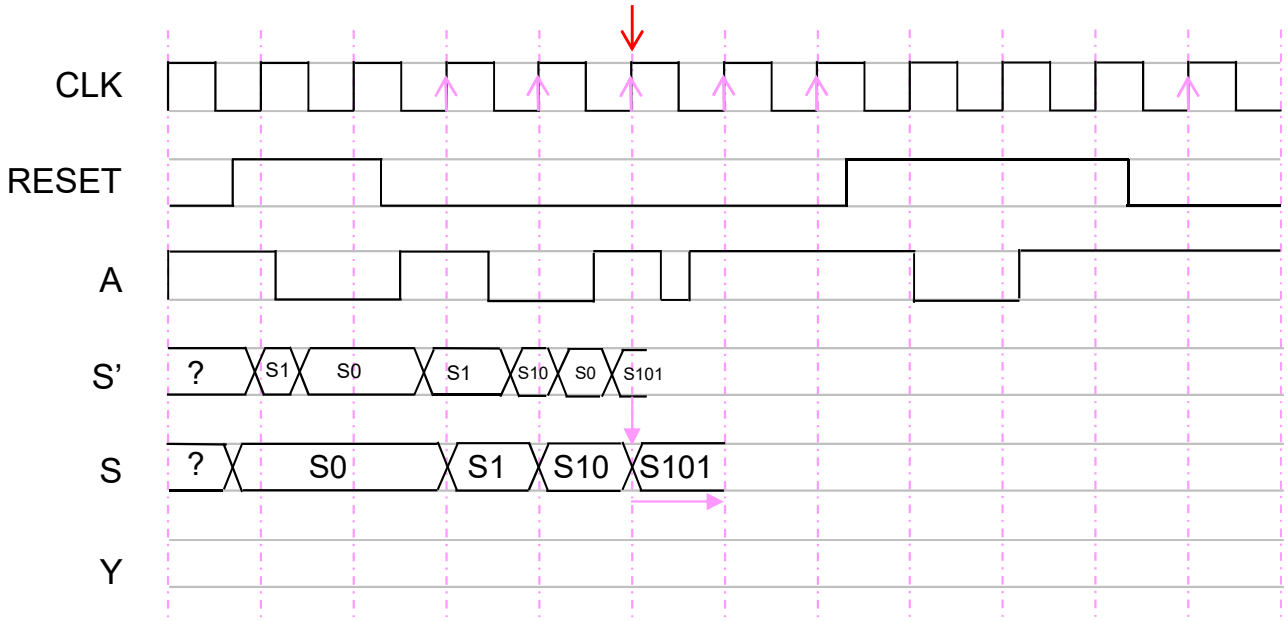

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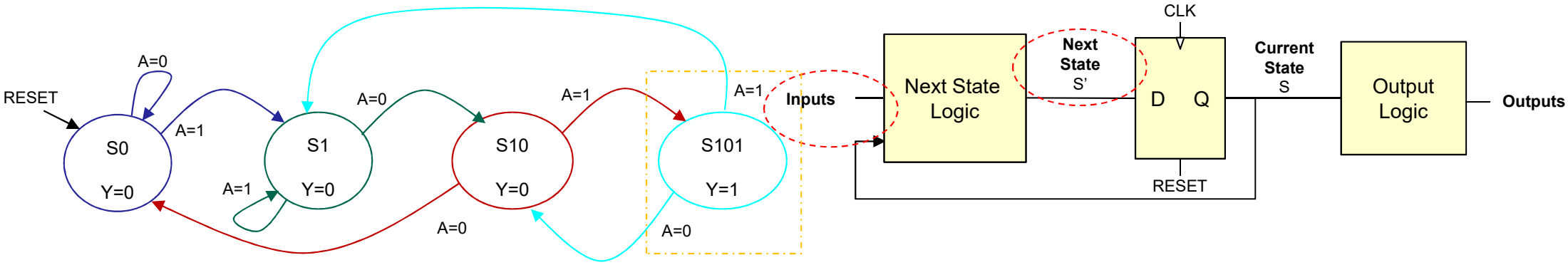

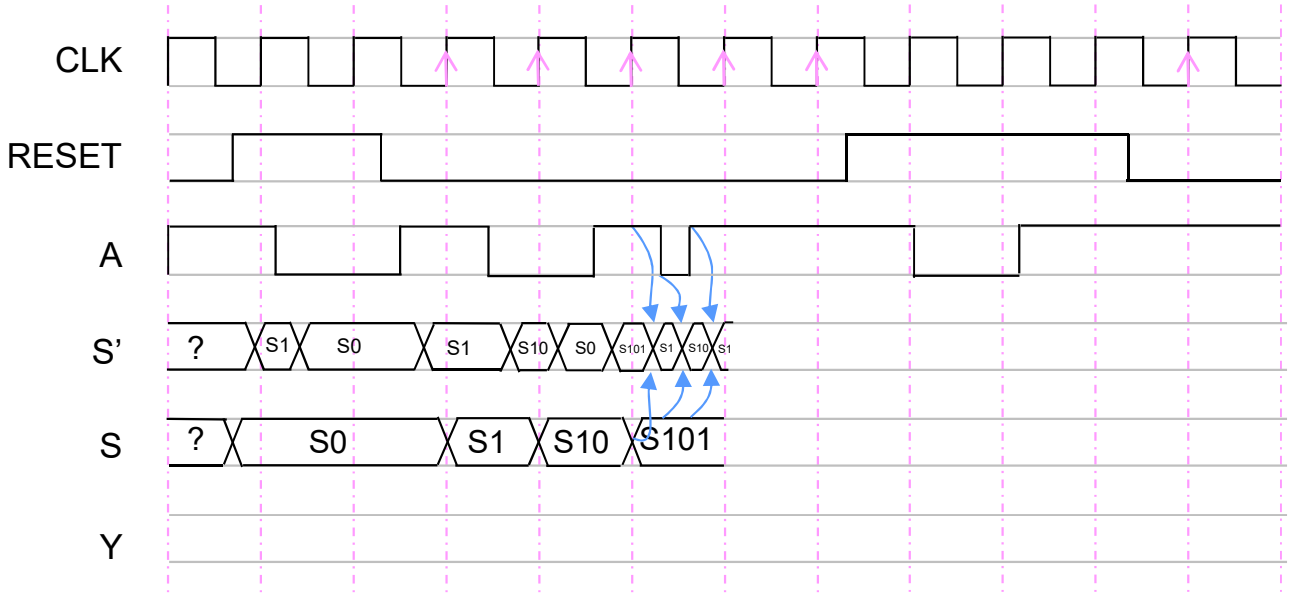

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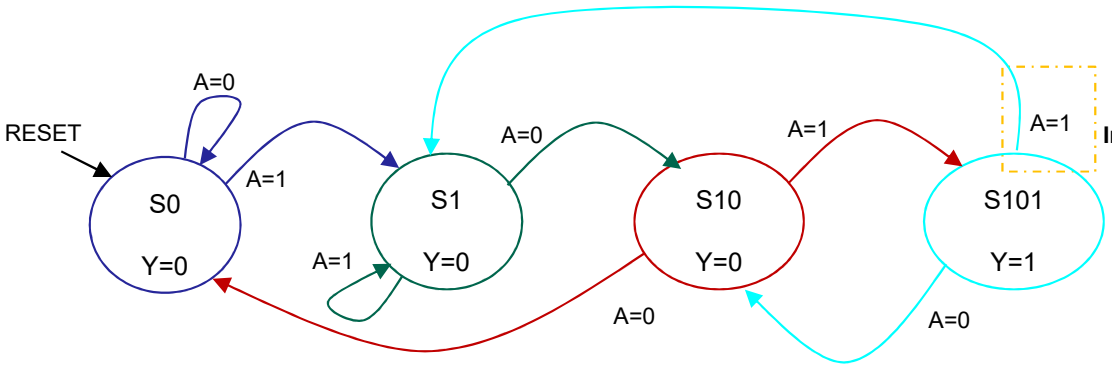

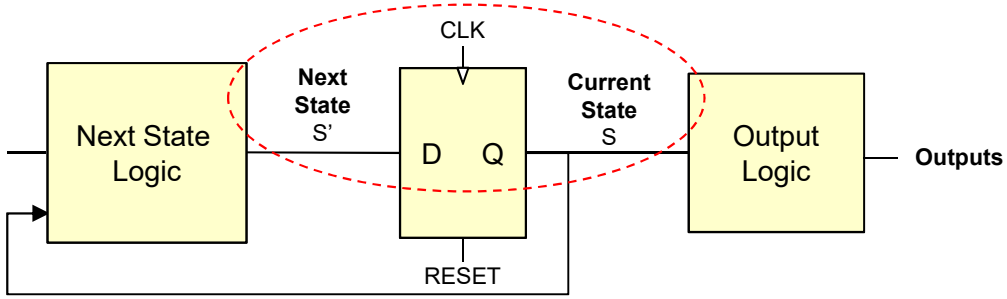

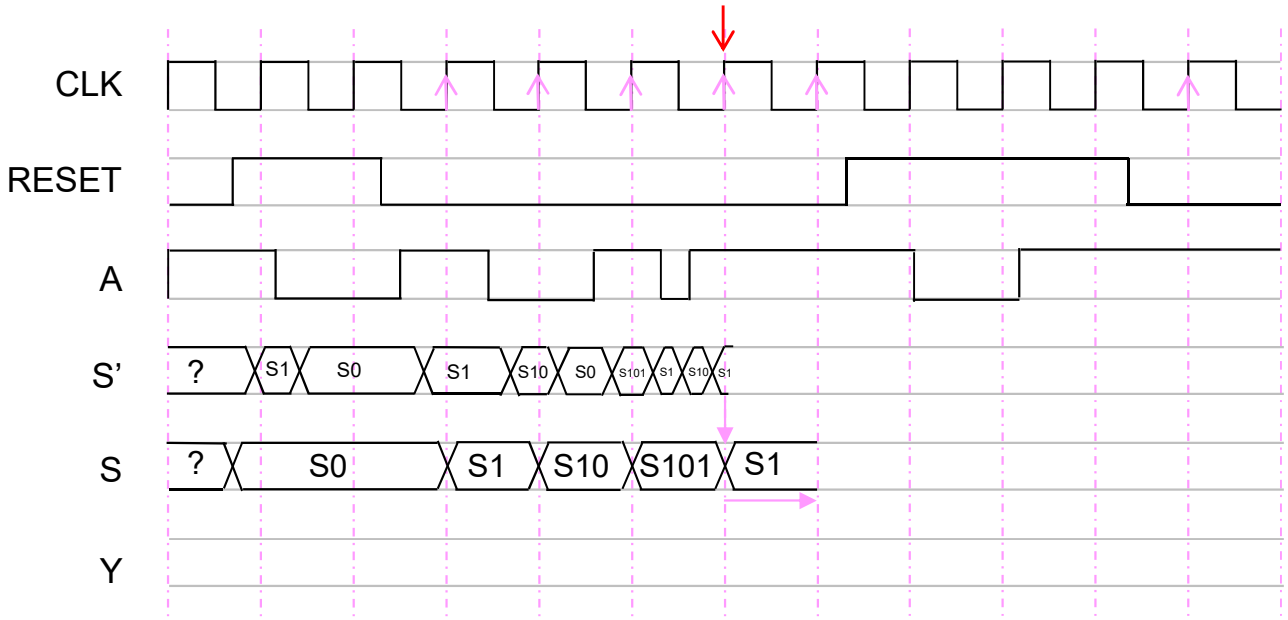

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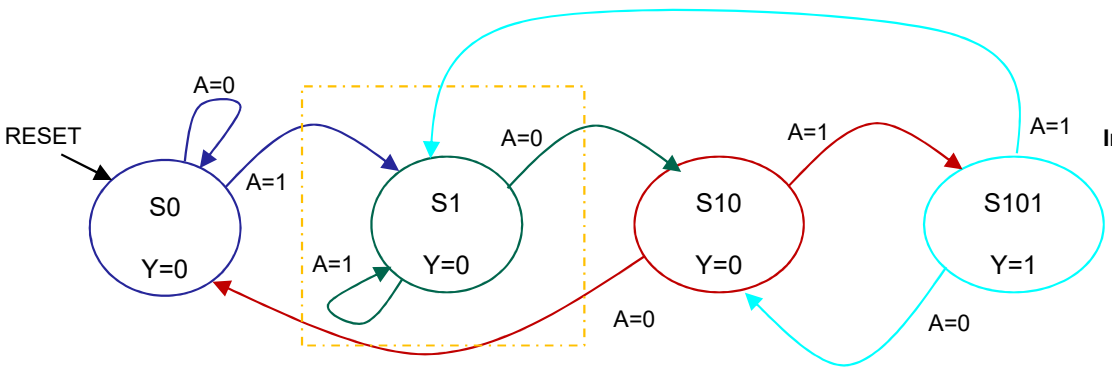

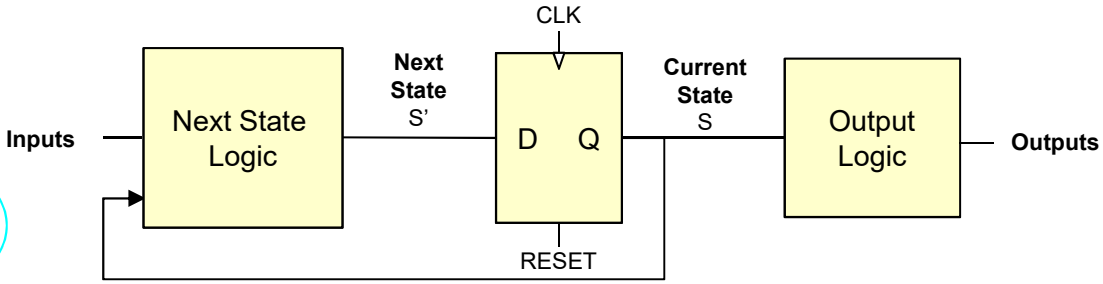

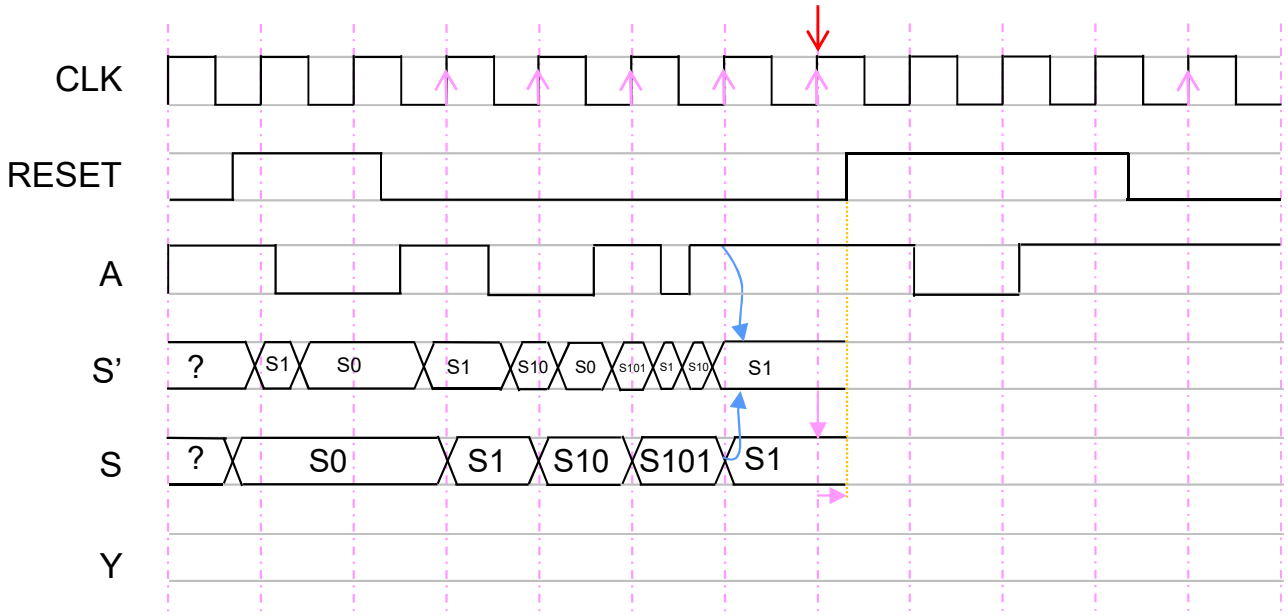

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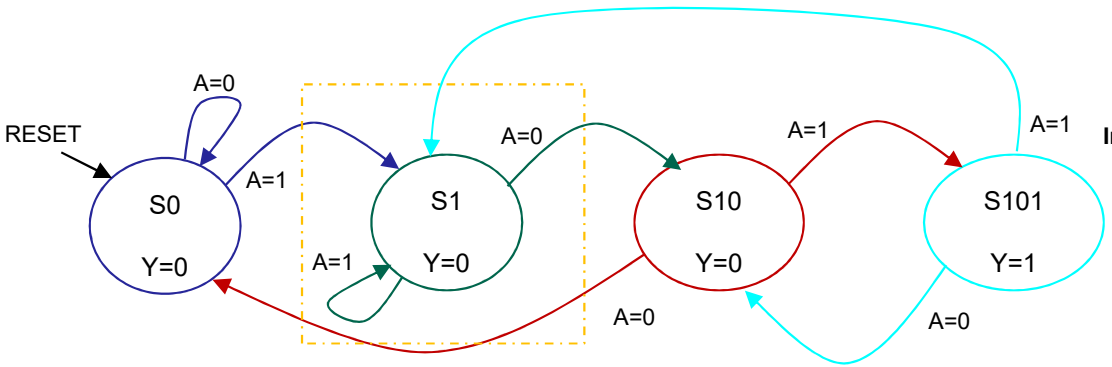
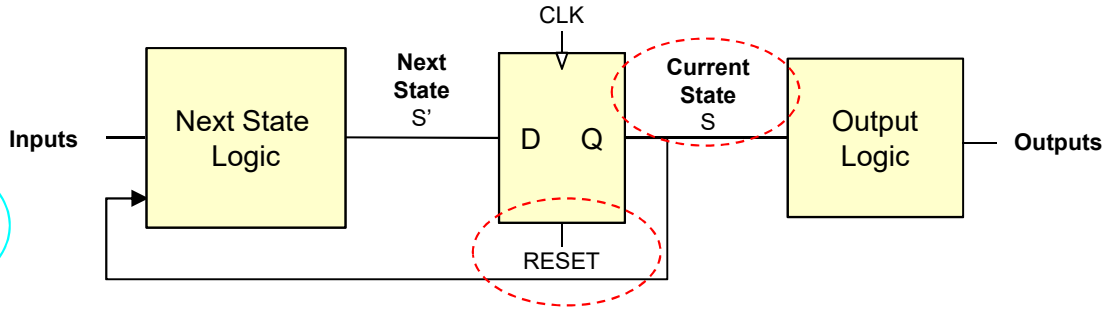
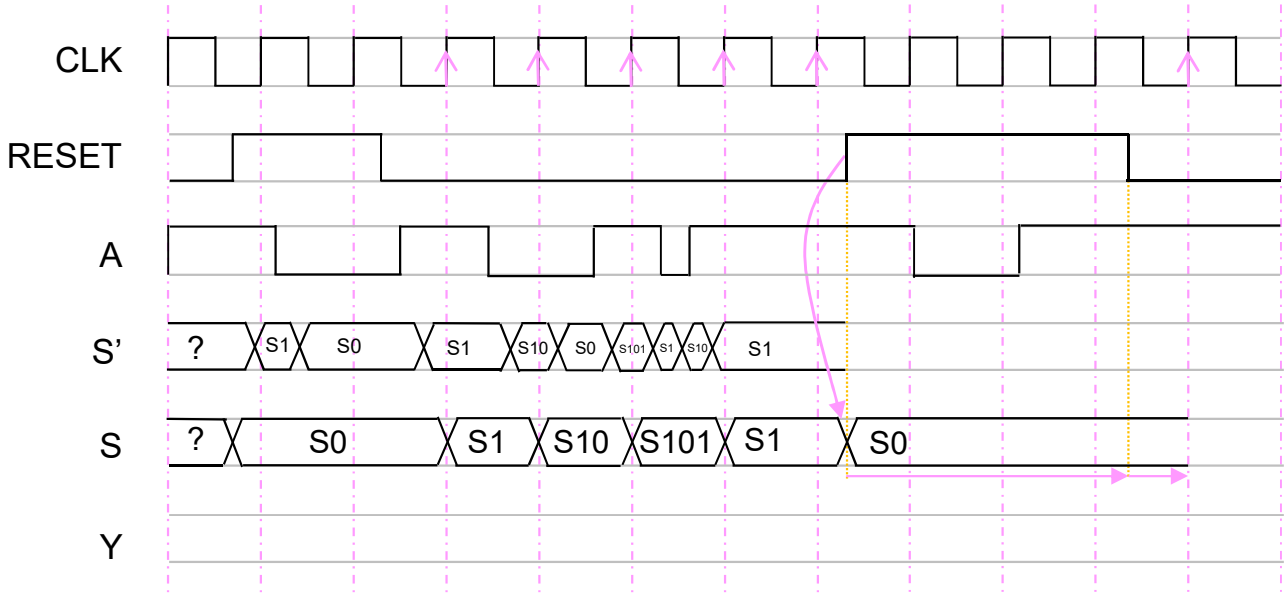
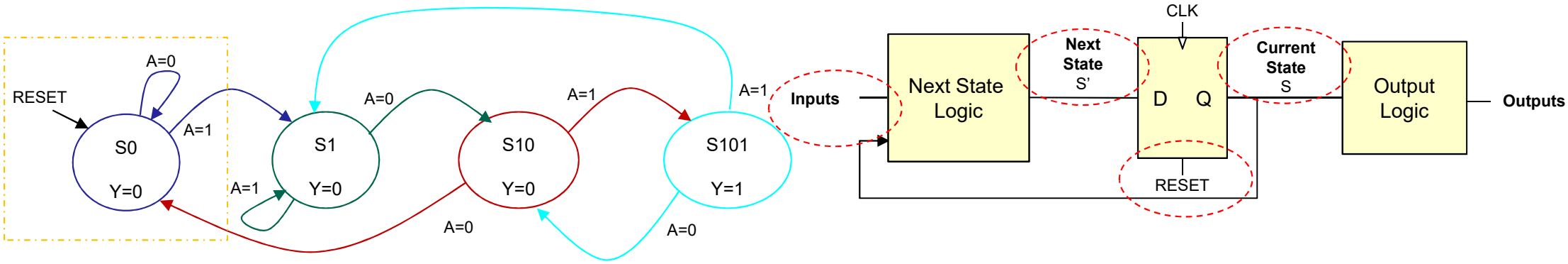
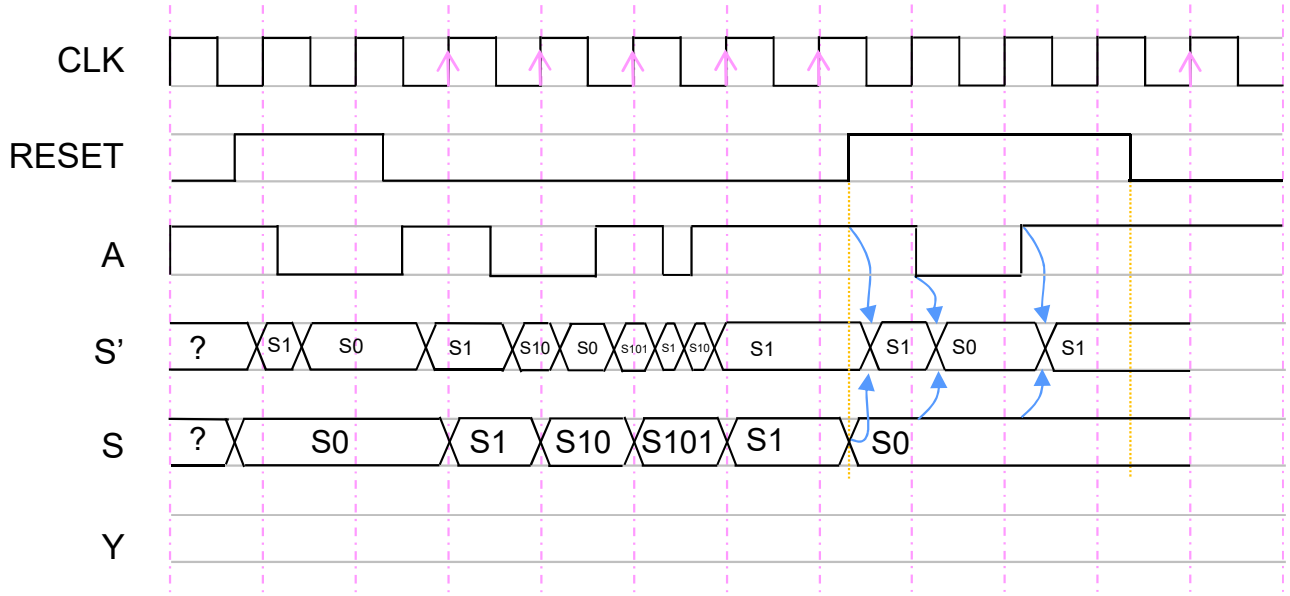




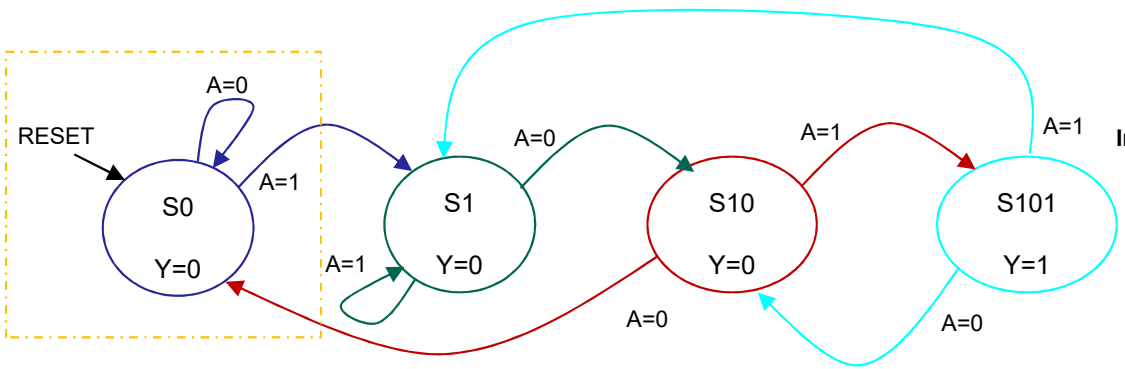


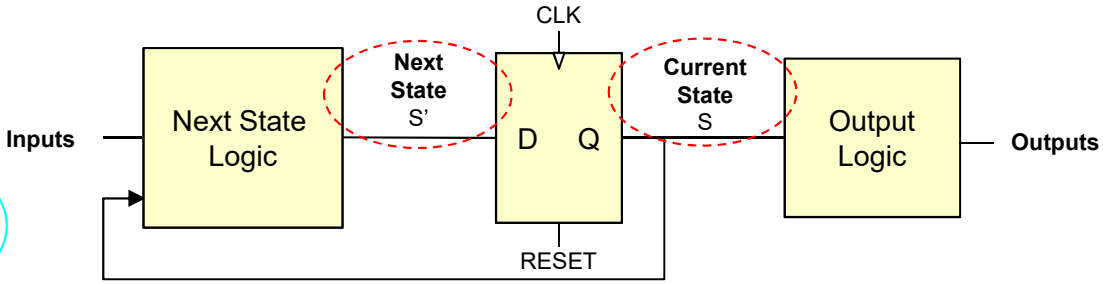
FSM Timing Diagram: Drawing the timing diagram

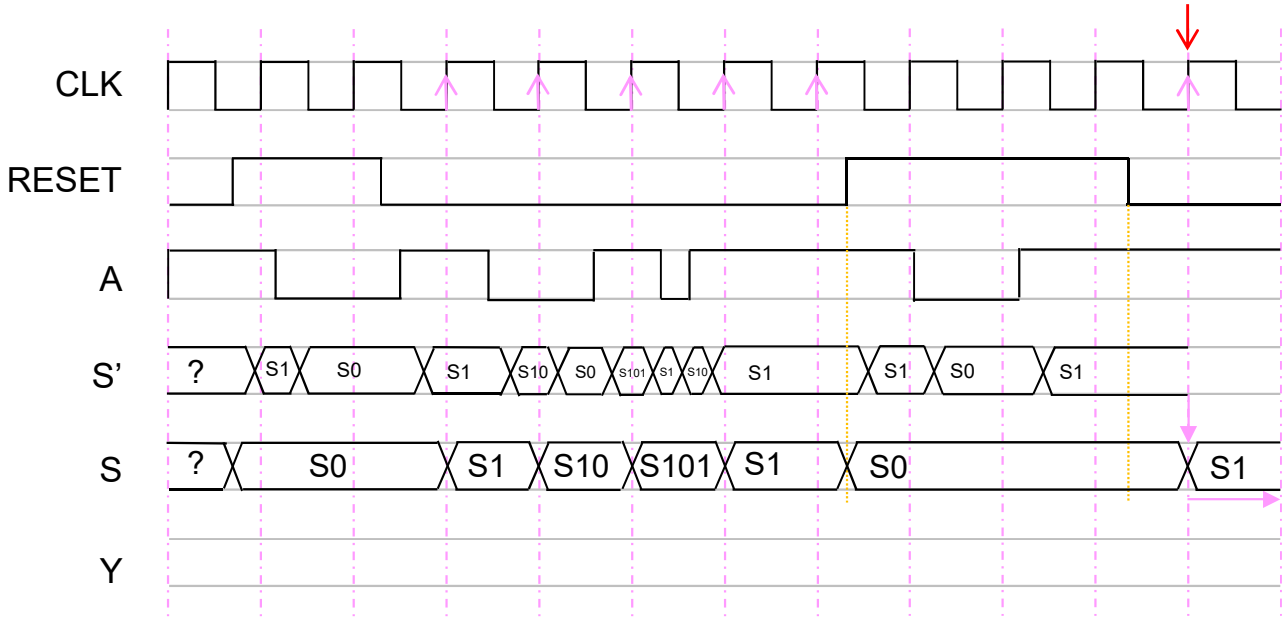




FSM Timing Diagram: Drawing the timing diagram







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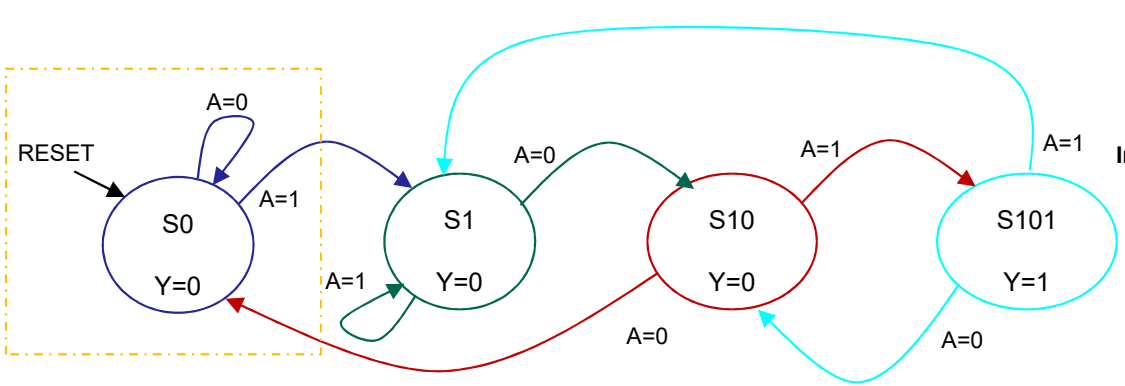

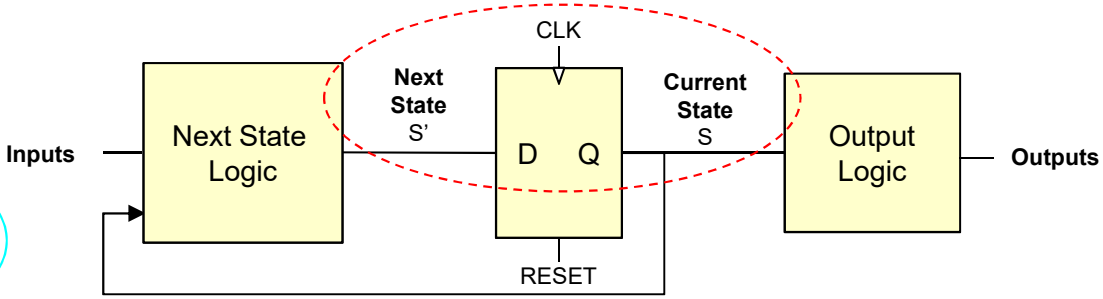

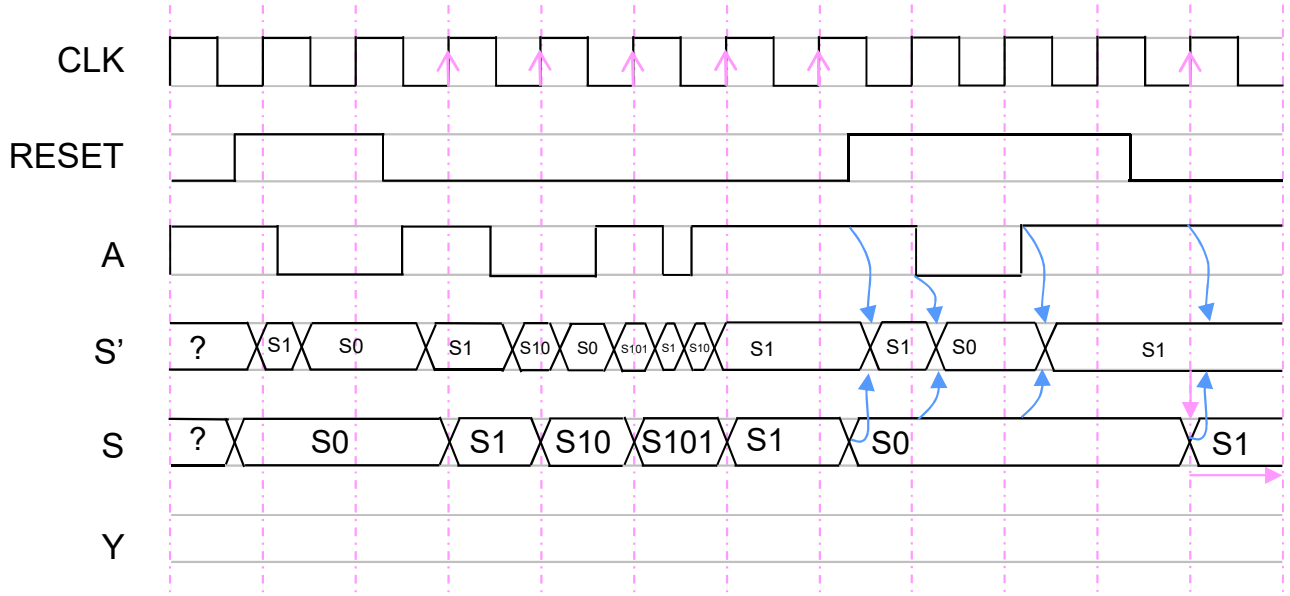

FSM Timing Diagram: Drawing the timing diagram